Remarks

The Final Office Action dated May 14, 2009, lists the following new grounds of rejection: claims 1-3, 5-10, 12 and 14-15 stand rejected under 35 U.S.C. § 103(a) over Huijsing (U.S. Patent No. 4,555,673) in view of Schade (U.S. Patent No. 4,392,112); claims 4 and 13 stand rejected under 35 U.S.C. § 103(a) over the '673 and '112 references in view of Miyazawa (U.S. Patent Pub. 2002/0196247); claim 11 stands rejected under 35 U.S.C. § 103(a) over the '673 reference in view of the '112 reference and Applicant Admitted Prior Art (AAPA). In this discussion set forth below, Applicant does not acquiesce to any rejection or averment in this Office Action unless Applicant expressly indicates otherwise.

Applicant respectfully traverses the § 103(a) rejections because the cited combination of references lacks correspondence. For example, neither of the asserted references teaches the claimed invention "as a whole" (§ 103(a)) including, *e.g.,* keeping the ratio of the transconductance of a NMOS transistor doublet and the transconductance of a PMOS transistor doublet constant. Because neither reference teaches these aspects, no reasonable combination of these references can provide correspondence. As such, the § 103 rejection fails.

More specifically, the '673 reference does not teach keeping the ratio of the transconductances of differential input portions 20 and 22 (*i.e.,* the asserted NMOS and PMOS doublets) constant, as claimed, but instead teaches controlling the transconductance of the differential amplifier that includes the differential input portions 20 and 22. *See, e.g.,* Figure 2. For example, the '673 reference discusses controlling the transconductance of the differential amplifier to be largely constant while failing to make any mention of the transconductances of differential input portions 20 and 22 relative to each other (*i.e.,* the ratio of their transconductances). *See, e.g.,* the Abstract and Col. 2:40-49.

In addition, the cited combination further fails to correspond to aspects of the claimed invention directed to selectively directing input signals only to the differential input of one of the NMOS and PMOS doublets and connecting the differential input of the other one of the NMOS and PMOS doublets to a reference voltage. The Office Action acknowledges that the '673 reference does not teach connecting input signals to

only one of the differential input portions 20 and 22 (*i.e.,* the asserted NMOS and PMOS doublets) since the '673 reference requires that voltages V_{I+} and V_{I-} be connected to both of the differential input portions 20 and 22. The '112 reference also fails to teach such aspects. In particular, the '112 reference does not even teach NMOS and PMOS doublets that each have a differential input. Instead, the '112 reference teaches that transistors Q3 and Q4 have a common base connection 18 (*i.e.,* these transistor do not have a differential input). *See, e.g.,* Figure 1 and Col. 3:44-53. As the '112 reference does not teach two transistor doublets that each have a differential input, the '112 reference does not teach connecting one of the differential inputs to input signals and connecting the other (nonexistent) one of the differential inputs to a reference voltage. Because neither reference teaches these aspects of the claimed invention, no reasonable combination of these references can provide correspondence.

Moreover, Applicant submits that the '673 reference teaches away from the Examiner's proposed combination. Consistent with the recent Supreme Court decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main ('673) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007) ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious."). In this instance, the '673 reference requires that voltages V_{I+} and V_{I-} be connected to both of the differential input portions 20 and 22. *See, e.g.,* Figure 2 and Col. 4:12-16 and Col. 4:54 to Col. 5:10. Specifically, the '673 reference requires that the differential input portions 20 and 22 both amplify the input signal in order for the amplifier to function in the intended manner. *See, e.g.,* Col. 3:3-50. Thus, the '673 reference teaches away from connecting the input signal only to one of the differential input portions 20 and 22 as proposed by the Examiner.

In view of the above, the § 103(a) rejections are improper and Applicant requests that they be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Aaron Waxler, of NXP Corporation at (408) 474-9063 (or the undersigned).

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

By: _____
Name: Robert J. Crawford
Reg. No.: 32,122
651-686-6633
(NXPS.593PA)